Remarks

Responsive to the Office Action mailed May 18, 2004, Applicants cancel non-elected claims 4-11 and 26, reserving the right to pursue these claims as originally filed in a divisional application.

By the foregoing amendment, claims 12-24 and 27-33 are pending, with claims 12 and 27 being independent.

A. 35 U.S.C. Sec. 112

Claims 12-24 and 27-33 stand rejected under 35 U.S.C. Sec. 112 (second paragraph) on the basis that (a) it is not clear when the context switch occurs with respect to the return of requested data in claims 12 and 27, and (b) it is not clear how the thread identifier is generated and used in these same claims. Regarding (a), claims 12 and 27 are amended for clarity. Regarding (b), the claims recite the generation of a system bus operation that sends a formulated instruction, data and thread identifier to a device. Applicants respectfully submit that this limitation satisfies 35 U.S.C. Sec. 112 (second paragraph) in that the thread identifier is simply one form of information being sent by a controller to a device via a system bus operation. As such, the subject matter is particularly pointed out and distinctly claimed.

Applicants further note that the generation and use of thread identifiers are well known to those having ordinary skill in the relevant art. The application describes an exemplary embodiment of a thread identifier which, according to such embodiment, is added to outgoing transactions of a processor by a bus controller (Application, p. 6, lns. 10-12), is an indicator of, among other things, the context number of the originating thread (Id.), and is used, for example, to ensure that data is returned to its intended destination (Application, p. 10, lns. 9-11 and p. 7, lns. 14-16).

In light of the foregoing, Applicants respectfully request reconsideration and withdrawal of the rejections of claims 12-24 and 27-33.

B. 35 U.S.C. Sec. 102(b)

Claims 12 and 27 stand rejected under 35 USC 102(b) as being anticipated by US Patent No. 5,421,014 ("Bucher"). Applicants respectfully traverse this rejection since Bucher neither suggests nor discloses a single instruction that requests a device to both perform a command and return data to a context-associated register.

Amended claims 12 and 27 recite in pertinent part:

Claim 12:
"a processor configured to formulate an instruction and data, from a thread associated with a first context, for sending to a device, **said instruction requesting the device to perform a command and write return data to a destination register associated with the first context in the processor**"

Claim 27:
"formulating, in a processor, an instruction and data from a thread associated with a first context for sending to a device, **the formulated instruction requesting the device to perform a command and write return data to a destination register associated with the first context in the processor**"

The foregoing claim language recites a single instruction that not only commands a device to perform an operation but also instructs the device to return data to the processor at a location associated with the originating context. As such, the claimed system and method require no second operation to return a value to a given thread for further processing. Certain advantages provided by such an instruction are noted in the Application at page 1, lines. 3-12:

> The performance of conventional processors in network communication systems is degraded by long latency accesses, especially to shared resources. For example, in order to look up data in a table lookup unit, a processor must send an operation with data to the table lookup unit (TLU) commanding the TLU to look up data in a table. After performing the lookup operation, the TLU stores the resulting data internally. The processor sends a load command requesting that the TLU load the result on the bus and return the data to the processor. This procedure requires two bus transactions initiated by the processor. Therefore, it would be desirable to have a single transaction both command the device to perform an operation and provide the result to the processor.

In contrast with the claimed subject matter, Bucher suggests and describes a processor or "initiator" that requires a two step execution and retrieval process analogous to the prior art described above. More specifically, when communicating with target devices, Bucher requires that (1) commands be issued to the targets and (2) results be retrieved. This process is set out in steps 12 and 16 of Fig.1, steps 34 and 36 of Fig. 2, the code in Figs. 6a and 6b and supporting text. Although it is unclear from the patent whether results are "retrieved" from a target (controller), devices hanging off of the target (see, e.g., Fig, 7) or an initiator (computer), a separate retrieval operation is nevertheless required to make use of the resulting data. As such, Bucher neither discloses nor suggests a system or method that uses a single instruction issued by a processor and associated with a first context to both (1) request a device to perform a command and (2)

write return data to a destination register within the processor where such register is associated with the first context.

In light of the foregoing, Applicants respectfully request reconsideration and withdrawal of the rejections of claims 12 and 27. All claims depending therefrom are also patentable over Bucher for at least the reasons noted above. As such, Applicants respectfully request reconsideration and allowance of all pending claims.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Respectfully submitted,

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